UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,938	12/08/2003	Sachiko Nemoto	5243-002-US01	8989

79184   7590   09/16/2008

HANIFY & KING PROFESSIONAL CORPORATION
1875 K STREET, NW
SUITE 707
WASHINGTON, DC 20006

EXAMINER
RIVAS, SALVADOR E

ART UNIT	PAPER NUMBER
2619	

MAIL DATE	DELIVERY MODE
09/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _13 May 2008_.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-5_ is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-5_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _13 May 2008_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All   b)☐ Some * c)☐ None of:

         1.☐ Certified copies of the priority documents have been received.

         2.☐ Certified copies of the priority documents have been received in Application No. _____.

         3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
     Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.　　This Action is in response to Applicant's amendments filed on April 21, 2008.

Claims 1-5 are now pending in the present application. **This Action is made Final**.

Drawings

2.　　The drawings were received on May 13, 2008. These drawings are acceptable.

Claim Rejections - 35 USC § 103

3.　　The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of

the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g)

prior art under 35 U.S.C. 103(a).

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

　　　　1.　　Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gonda (U.S. Patent Application Publication # 2003/0056017 A1)** in view of **Zelig et al. (U.S. Patent Application Publication # 2002/0110087 A1)**, and further in view of **Yu (U.S. Patent Application Publication # 2001/0043603 A1)**.

Regarding **claim 1**, Gonda teaches an interface device (read as translation engine, paragraph [0012], Line 1), comprising:

an Ethernet frame and a SONET frame convertible interface device (the translation engine performs the function of "translating Ethernet frames to SDH/SONET frames and vice versa.", paragraph [0012], Line 2-3),

wherein a 1st holding part (read as buffer (Fig.1 @ 103)) with a specific VLAN identifier of said Ethernet frame and a STS path identifier of said SONET frame are placed opposite each other. (read as the buffer holds "… Ethernet frames. An Ethernet MAC address is provided for a corresponding SDH/SONET TDM slot.", paragraph [0017], Line 4-6) and

However, Gonda et al. fails to teach a multiplexing part operable to multiplex an Ethernet frame having said specific VLAN identifier corresponding to said specific STS path identifier that is held by said 1st holding part among a plurality of input Ethernet frame VLAN identifiers.

Zelig et al. teaches a multiplexing part (read as switch labeled "MUX A" (Fig.1 @ 26)) capable of multiplexing an Ethernet frame having said specific VLAN identifier

(MUX A "multiplexes ... different Ethernet ports 28 of the switch and having different

VLAN addresses 30", paragraph [0052], Line 10-12) corresponding to said specific STS

path identifier that is held by said 1st holding part among a plurality of input Ethernet

frame VLAN identifiers ("Switch 26 now registers the requested service in a service

table it maintains and sends a signaling message regarding the service ..." (paragraph

[0055], Line 1-3) which may contain the type of service (e.g. SONET over MPLS)

and/or may contain an "additional index ... to the signaling message to specify the

range of VLANs for Ethernet services, or the number of the SONET path for SONET

signals at both ends of the connection" (paragraph [0055], Line 16-20)). It would have

been obvious to a person of ordinary skill in the art to combine Zelig et al. with Gonda

for the purpose of mapping data packets to a STS channel for transmission. The

motivation to combine is to efficiently map a plurality of Ethernet frames to a one STS

signal and vice versa.

However, Gonda et al. and Zelig et al. wherein the multiplexing part establishes a

filtering part that passes through Ethernet frames having a specific VLAN identifier

among a plurality of Ethernet frames and

a 1st encapsulating part that encapsulates information data contained in an

Ethernet frame that passes through a filtering part.

Yu teaches a transmission method and apparatus (Fig.9) for "... transmitting data

packets from an upper layer side device to a lower layer side device." (Paragraph [0022]

Lines 1-3) Furthermore, Yu teaches wherein the multiplexing part establishes a filtering

part (read as a packet adapt function) that passes through Ethernet frames having a

specific VLAN identifier among a plurality of Ethernet frames ("receiving and buffering

the data packets from said upper layer side device, adapting the rate of said upper layer

side device to the rate of said lower layer side device, ..." Paragraph [0022] Lines 4-7)

and

a 1st encapsulating part that encapsulates information data contained in an

Ethernet frame that passes through a filtering part.("encapsulating said first type of

frames to form a second type of frames containing a SAPI field including a SAPI

identifier and an information field including said data packets;" Paragraph [0022] Lines

8-10)

Therefore, it would have been obvious to a person of ordinary skill in the art at

the time the invention was made to include the functions for adapting and encapsulating

a data packet as taught by Yu and the VLAN ID mapping table as taught by Zelig et al.

to modify the interface system taught by Gonda et al. for the purpose of efficiently

mapping a plurality of Ethernet frames to a one STS signal and vice versa.

Regarding **claim 2**, and **as applied to claim 1 above**, Yu, as modified by Gonda

et al. and Zelig et al., teach an interface device (read as ADM (Fig.9, Fig.15)) wherein

the multiplexing part establishes an ID inserting part that inserts an opposing SONET

transmission device STS path identifier that opposes an Ethernet frame that is

encapsulated by a 1st encapsulating part (Paragraph [0022] Lines 8-10).

Regarding **claim 3**, Yu, as modified by Gonda et al. and Zelig et al., teach a

SONET multiplex isolation device (read as ADM (Fig.9, Fig.15)) wherein the

multiplexing part establishes a flag inserting part that inserts a flag that indicates an

input side Ethernet frame transmission fault in an Ethernet frame that is encapsulated

by a 1st encapsulating part (Paragraph [0020] Lines 16-20, Paragraph [0119]).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Yu (U.S.**

Patent Application Publication # 2001/0043603 A1) in view of **Kong et al. (US**

Patent # 2002/0176450 A1).

Regarding **claim 4**, Yu teaches a transmission system (Fig. 15) (read as a

transmission method and apparatus for "… transmitting data packets from an upper

layer side device to a lower layer side device." Paragraph [0022] Lines 1-3), comprising:

a plurality of SONET multiplex isolation devices (read as ADM devices (Fig.9,

Fig.15)) having Ethernet interface devices (Paragraph [0014]) and SONET interface

devices (Paragraph [0015]) established (Paragraph [0083]),

wherein a 1st SONET multiplex isolation device (Fig.15) among the plurality of

SONET multiplex isolation devices (read as ADM devices (Fig.9, Fig.15)) establishes a

1st holding part (read as a buffering device (Fig.9 @ 8, 13)) with a Ethernet frame

specific VLAN identifier and a SONET frame specific STS path identifier placed

opposite each other ("… receiving and buffering the data packets from said upper layer

side device, adapting the rate of said upper layer side device to the rate of said lower

layer side device, …" Paragraph [0022] Lines 4-7);

a multiplexing part (Fig.9, Fig.13) that multiplexes a plurality of Ethernet frames

having a specific VLAN identifier corresponding to the specific STS path identifier that is

held in the 1st holding part (read as FIFO (Fig.9 @ 8, 13)) among an input plurality of

Ethernet frame VLAN identifiers ("converting said data packets to a first type of frames;"

Paragraph [0022] Lines 4-7),

along with a 2nd SONET multiplex isolation device (read as ADM (Fig.15))

among the plurality of SONET multiplex isolation devices (read as ADM (Fig.9, Fig.15))

with a 2nd holding part (Fig.9 @ 8, 13) with the SONET frame specific STS path

identifier and Ethernet frame specific VLAN identifier placed opposite each other ("...

apparatus for providing a point-to-point full-duplex simultaneous bi-directional operation

for connecting physical layer side device and network layer side device, for example,

connecting Ethernet Switches and a SDH/SONET network." Paragraph [0019] Lines 2-

6); and

wherein the 1st SONET multiplex isolation device (read as an ADM (Fig.9,

Fig.15)) multiplexing part inserting a flag that indicates an input side Ethernet frame

transmission fault along with the 2nd SONET multiplex isolation device isolation part

(read as an ADM (Fig.9, Fig.15)) that prevents output of an Ethernet frame that is

transmitted by detection of the flag from a frame originating in the SONET frame ("For

the purpose of determining whether or not the bit error rate of the received signal is

above or below two different provisionable thresholds, the EOS apparatus provides two

B2 error rate threshold blocks. The Signal Fail (SF) and the Signal Degrade (SD)

conditions are reported when thresholds are exceeded via interrupts." Paragraph

[0119]).

However, fails to teach an isolation part that imparts a VLAN identifier

corresponding to the STS path identifier that is held in the 2rid holding part to each

extracted Ethernet frame by extracting each Ethernet frame and the SONET frame STS

path identifier from a frame originating in the SONET frame

Kong et al. teach mapping mechanisms (Fig.3) ("... tagged method of the

Ethernet frame using VCL or VLAN tag (see FIG. 6)" (paragraph [0059], Lines 19-21)

that may be applied as an "... index variable in a table that will provide the channel

number ..." (paragraph [0062], Lines 13-14)) to establish a communication path to carry

Ethernet signals over a SONET/SDH network (Paragraph [0014]). Furthermore, Kong et

al. teach an isolation part that imparts a VLAN identifier corresponding to the STS path

identifier that is held by the 2nd holding part to an extracted plurality of Ethernet frames

by extracting each Ethernet frame and the SONET frame STS path identifier from a

frame originating in SONET frames with a multiplexed plurality of Ethernet frames

("...mapping mechanisms in FIG. 3 works for traffic flowing in both directions. The key

for the inverse mapping from SONET payload to Ethernet ports is to map SONET signal

correctly to a Ethernet port.", paragraph [0062], Lines 1-4).

Therefore, it would have been obvious to a person of ordinary skill in the art at

the time the invention was made to include the VLAN tagging and mapping mechanisms

applied to Ethernet frames as taught by Kong within the ADM devices as taught by Yu

for the purpose of efficiently establishing communication between a telecom

SDH/SONET transmission device and a remote access datacom device by adapting

MAC frame directly to SDH/SONET and vice versa.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Yu (U.S.**

Patent Application Publication # 2001/0043603 A1) in view of **Zelig et al. (U.S.**

Patent Application Publication # 2002/0110087 A1).

Regarding **claim 5**, Yu teaches a frame transmission method for frame

transmission for an Ethernet flame and SONET frame (Fig.9), except for inputting a

plurality of Ethernet frames having a specific VLAN identifier among the plurality of

Ethernet frames passes through to be multiplexed.

Zelig et al. teaches a multiplexing part (read as switch labeled "MUX A" (Fig.1 @

26)) capable of multiplexing an Ethernet frame having said specific VLAN identifier

(MUX A "multiplexes … different Ethernet ports 28 of the switch and having different

VLAN addresses 30", paragraph [0052], Line 10-12) corresponding to said specific STS

path identifier that is held by said 1st holding part among a plurality of input Ethernet

frame VLAN identifiers ("Switch 26 now registers the requested service in a service

table it maintains and sends a signaling message regarding the service …" (paragraph

[0055], Line 1-3) which may contain the type of service (e.g. SONET over MPLS)

and/or may contain an "additional index … to the signaling message to specify the

range of VLANs for Ethernet services, or the number of the SONET path for SONET

signals at both ends of the connection" (paragraph [0055], Line 16-20)).

Therefore, it would have been obvious to a person of ordinary skill in the art at

the time the invention was made to include the VLAN ID session map as taught by Zelig

et al. within the transmission apparatus of Yu for the purpose of transmitting data

packets from an upper layer side device to a lower layer side device. (Paragraph [0022] Lines 1-3).

Response to Arguments

4.   Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: **Goody (U.S. Patent # 7,031,324 B1)**, **Ueno et al. (U.S. Patent Application Publication # 2003/0117952 A1)**, **Morita et al. (U.S. Patent Application Publication # 2003/0076857 A1)**, **Jordan (U.S. Patent Application Publication # 2003/0016697 A1)**, and **Hosler et al. (U.S. Patent # 7,031,252 B1)**.

        THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

        A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

>   Commissioner for Patents
>   P.O. Box 1450
>   Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

>   Customer Service Window
>   Randolph Building
>   401 Dulany Street
>   Alexandria, VA 22314

Any inquiry concerning this communication or early communications from the Examiner should be directed to Salvador E. Rivas whose telephone number is (571) 270-1784. The examiner can normally be reached on Monday-Friday from 7:30AM to 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Chirag G. Shah can be reached on (571) 272- 3144. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Salvador E. Rivas
S.E.R./ser

September 4, 2008

/Chirag G Shah/

Supervisory Patent Examiner, Art Unit 2619